Electronic Version
Stylesheet Version v1.1.1

# [High-Voltage Input Tolerant Receiver]

## Abstract

A high-voltage input tolerant receiver capable of achieving power savings with less distortion of analog signals is disclosed. When an external signal ϕC input from a PAD 2 is less than 3.6V, a p-channel MOS transistor P10 is turned off. As a result, a control signal ϕE becomes 0V to turn on a p-channel MOS transistor P1. At this time, an intermediate signal ϕD output from a clamp circuit 3 becomes equivalent to the external signal ϕC, and is not distorted. However, when the external signal ϕC exceeds 3.6V, the p-channel MOS transistor P10 is turned on, and a control signal ϕF output from a differential amplifier 9 becomes 0V. As a result, the p-channel MOS transistor P1 is turned off, and a level keeper 6 is enabled. Since the level keeper 6 remains inactive until the external signal exceeds 3.6V, current flowing through the level keeper 6 can be reduced.